

# Efficient circuit design for low power energy harvesting

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## ABSTRACT

We present five circuit topologies for low power energy harvesting. The most efficient circuit uses a variable capacitor as the power source, a DC bias voltage to charge the variable capacitor, two transistors for rectification, and two storage capacitors. Varying the capacitance performs work and results in stored charge in the capacitors. We experimentally measure the storage capacitor voltage and current over time. The circuit efficiency nears 50% at a maximum power of 10 nW. Multiple circuit topologies are simulated and yield efficiencies from 15% to 50%.

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## I. INTRODUCTION

Recent developments in ultra-low power consuming circuit designs have reduced power demand to picowatts in the standby mode, nanowatts in the active mode, and operation on an ultra-low duty cycle.<sup>1</sup> These breakthroughs make possible the use of ambient vibrations as a power source, *in lieu* of batteries.<sup>2–4</sup> Correspondingly, there is active interest in developing systems that harvest energy from the environment.<sup>5–8</sup> One aim of this research is to rectify low currents while maintaining a high efficiency. The goal is not only to optimize the power harvested but also to maximize the energy conversion efficiency.<sup>9,10</sup>

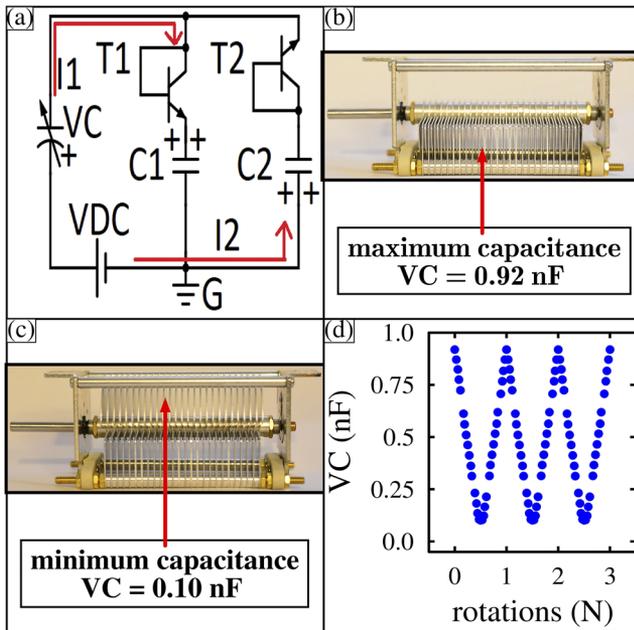
Generally, four mechanisms for energy harvesting exist: electromagnetic, magneto-strictive, piezoelectric, and electrostatic.<sup>11–23</sup> Electrostatic circuits have been proposed for wind farm power plants, as they can operate at extremely high voltages.<sup>24–26</sup> At the other end of the spectrum, electrostatic generators are compatible with microelectromechanical systems (MEMSs), are easy to construct, and can be made smaller than batteries.<sup>27–29</sup>

Electrostatic circuits typically use a variable capacitor to generate power, which must be either internally or externally polarized. When an external DC source is used, this power source does not contribute to the energy harvested.

In this study, we use a circuit similar in design to that used by Philp<sup>25</sup> and O'Donnell,<sup>26</sup> but for high-efficiency low power energy harvesting. First, we present a circuit that uses a variable capacitor charged with a DC voltage source to convert mechanical energy to stored electrical energy. Second, we present an equivalent circuit that uses a fixed capacitor with an AC voltage source but allows us to measure the efficiency. Third, we present simulation results for various circuit topologies and report their power production and efficiency.

## II. DC EXPERIMENTAL METHOD, RESULTS, AND DISCUSSION

The most efficient energy harvesting circuit we studied is shown in Fig. 1(a). The circuit has a variable capacitor (VC), a DC voltage source  $V_{DC}$ , two transistors  $T_1$  and  $T_2$  for rectification, and two storage capacitors  $C_1$  and  $C_2$ . The VC has both movable and fixed semi-circular plates. Its maximum capacitance occurs when the plates are aligned, as shown in Fig. 1(b). Its minimum capacitance occurs when the plates have no overlap, as shown in Fig. 1(c). As the plates rotate, the VC capacitance changes linearly from 0.92 nF to 0.10 nF and then back to 0.92 nF for each complete rotation, as



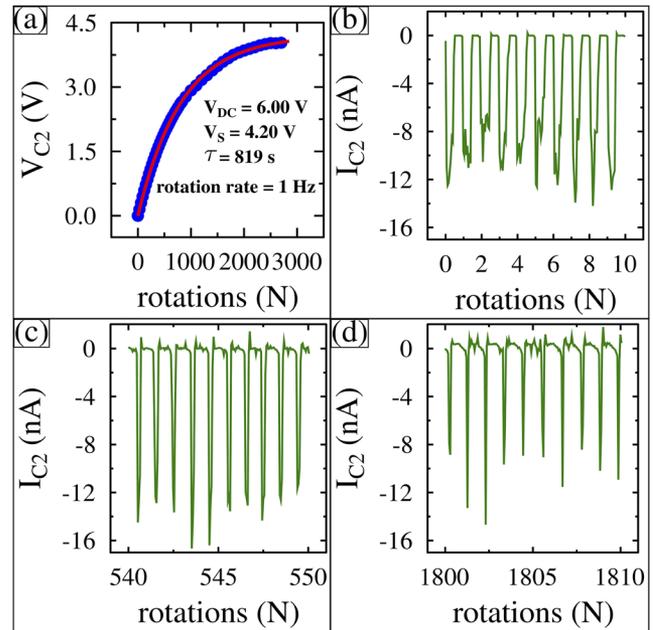
**FIG. 1.** (a) Schematic for the energy harvesting circuit. (b) Photograph of the variable capacitor at maximum capacitance. (c) Photograph of the variable capacitor at minimum capacitance. (d) Capacitance variation vs the number of 360° rotations.

shown in Fig. 1(d). This range of capacitance challenges the circuit design to be efficient at low currents.

Energy harvesting occurs when the VC is rotated. For example, as the VC capacitance increases under the influence of the constant DC voltage, charge will flow onto the VC. During this phase, the current  $I_1$  is generated and flows in a clockwise direction through  $T_1$  and charges the storage capacitor  $C_1$ . Similarly, as the VC capacitance decreases, charge will flow off the VC, opposite to the battery bias. If the battery is rechargeable, this will recharge the battery. During this phase, the current  $I_2$  is generated and flows in a counterclockwise direction through  $T_2$  and charges the storage capacitor  $C_2$ . Note that to achieve greater efficiency, we use transistors for rectification, instead of diodes, by connecting the base and collector together.

To test the circuit, we set the DC voltage to 6.0 V and rotated VC at 1 Hz. The voltage on  $C_2$  ( $V_{C2}$ ) was then measured as a function of the number of rotations  $N$ , as shown in blue in Fig. 2(a). The voltage increases continuously and saturates at  $V_S = 4.2$  V. The voltage on  $C_1$  was also measured, and it matches that on  $C_2$  (not shown). Note that it is not possible for the battery to contribute to  $V_{C2}$ .

The current flowing into  $C_2$  was also measured as a function of the VC rotations. In the early stages of charging (zero to ten rotations), the current oscillates at 1 Hz, as shown in Fig. 2(b). The maximum current is about 12 nA, and the width of each current spike is about half the cycle. As the number of rotations increases, the capacitor continues to charge and the height of the current spikes remains the same. However, the width of the current spikes decreases, as shown in Figs. 2(c) and 2(d). Thus, less current is flowing onto the capacitor as the number of rotations increases.



**FIG. 2.** (a) Measured voltage on  $C_2$  (blue) and fit (red). (b) Measured current flowing to  $C_2$  near  $V_{C2} = 0.00$  V, (c) near  $V_{C2} = 2.03$  V, and (d) near  $V_{C2} = 3.75$  V as a function of the rotation number for ten rotations.

Given that the voltage  $V_{C2}$  as a function of rotations in Hz is the same as time in seconds, we fit the voltage using the following function:

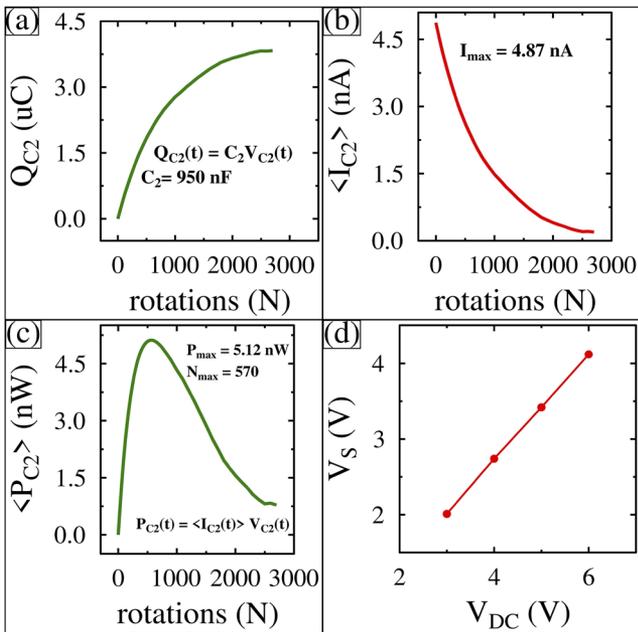
$$V_{C2}(t) = V_s \left( 1 - e^{-\left(\frac{t}{\tau}\right)} \right), \quad (1)$$

where  $\tau$  is the only fitting parameter and was found to be 819 s. The fit line is shown in red in Fig. 2(a).

Using the voltage data  $V_{C2}$  in Fig. 2(a), the charge stored on  $C_2$  as a function of time was calculated using  $Q = CV$  and is shown in Fig. 3(a). Next, the average current was calculated using  $I = dQ/dt$  and is shown in Fig. 3(b). The average current starts off at a maximum and decreases with time. This is consistent with the decreasing width of the current spikes shown earlier in Figs. 2(b)–2(d). The average power delivered to  $C_2$  as a function of time was calculated using the voltage data in Fig. 2(a) times the average current data in Fig. 3(b) and is shown in Fig. 3(c). The maximum power delivered to  $C_2$  is found to be 5 nW, and this occurs at 570 s. In order to determine the role of the DC power source, its value was varied from 3 V to 6 V in 1 V increments. Raising  $V_{DC}$  raises  $V_S$  in a linear manner, as shown in Fig. 3(d).

### III. AC EXPERIMENTAL METHOD, RESULTS, AND DISCUSSION

Next, we measured the performance of an equivalent circuit that uses an AC voltage source with a fixed capacitor (vs a DC source with a VC), as shown in Fig. 4(a). This circuit allows us to measure the amount of power coming from the power supply and thus determine the efficiency of the circuit.



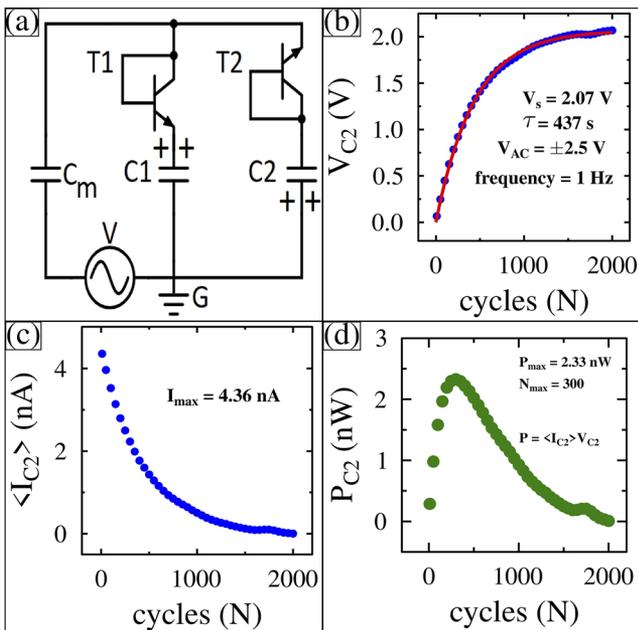
**FIG. 3.** (a) Charge, (b) average current, and (c) average power on  $C_2$  as a function of the rotation number (time in seconds). (d) Saturation voltage as a function of the applied DC bias voltage.

For this measurement, we set  $V_{AC}$  to be a 1 Hz sine wave with an amplitude of 2.5 V and no DC offset. We used a fixed capacitor,  $C_m = 1$  nF, and measured the voltage as a function of time in seconds on the storage capacitor  $C_2$ . Similar to the DC experimental results shown earlier, the voltage on  $C_2$  increases as a function of time and saturates at  $V_s = 2.07$  V, as shown in Fig. 4(b). The average current flow into  $C_2$  was calculated and is shown in Fig. 4(c). The average current starts off at a maximum value and decreases with time. The average power delivered to  $C_2$  was found by using the voltage in Fig. 4(b) and the average current in Fig. 4(c) and is shown in Fig. 4(d). Notice the output power increases to a maximum value of 2.5 nW before decreasing with time.

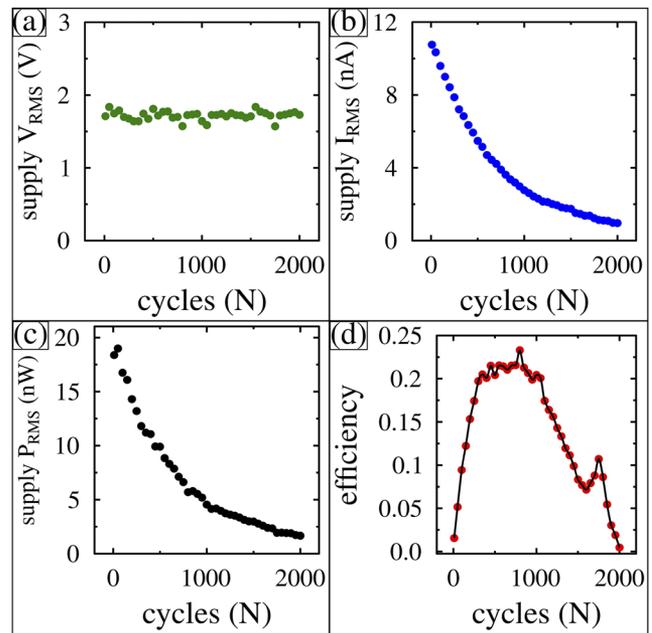
Throughout the charging of  $C_2$ , the voltage and current provided by the AC power source were also measured, as shown in Figs. 5(a) and 5(b), respectively. This is a constant voltage power source. The average power provided by the AC power source is shown in Fig. 5(c). Efficiency was found by dividing the power in Fig. 4(d) by the power in Fig. 5(c) and is shown in Fig. 5(d). The power delivered to  $C_2$  yields a maximum efficiency close to 25%. Given the same power is delivered to  $C_1$ , the circuit has an efficiency near 50%.

#### IV. SPICE SIMULATIONS, RESULTS, AND DISCUSSION

Power and efficiency simulations were run using the energy harvesting circuit shown in Fig. 4(a). The simulation predicts the voltage on  $C_2$  as a function of time (cycles). It also reports the power in the capacitors, the power delivered from the power supply, and efficiency. The simulations were run using  $V_{AC} = 2 \pm 1$  V (1 V sine



**FIG. 4.** (a) Schematic of the equivalent AC energy harvesting circuit. (b) Measured voltage on  $C_2$ , (c) calculated average current flowing into  $C_2$ , and (d) calculated average power delivered to  $C_2$  as a function of the cycle number (time in seconds).

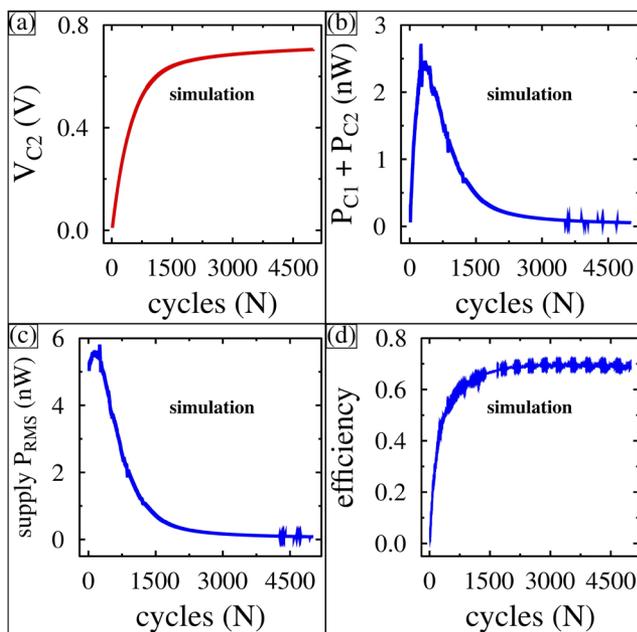


**FIG. 5.** (a) Measured output rms voltage from the AC power supply. (b) Output rms current from the AC power supply. (c) Output rms power provided to the circuit from the AC power supply. (d) Efficiency as a function of the cycle number (time in seconds).

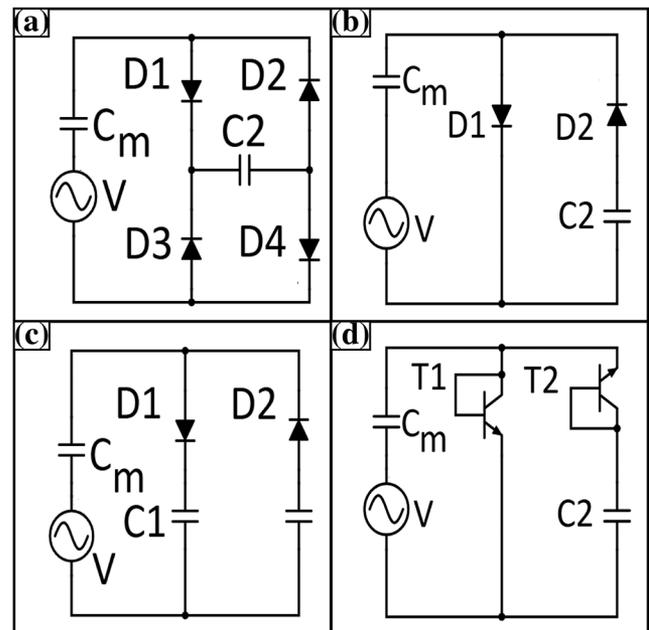
wave amplitude and 2 V DC offset),  $C_m = 1$  nF, and  $C_1 = C_2 = 1$   $\mu$ F. The voltage on  $C_2$  increases continuously in time and approaches a saturation value of about 0.7 V, as shown in Fig. 6(a). The power stored in both capacitors increases to a maximum value of 2.5 nW, as shown in Fig. 6(b). The power delivered to the circuit from the power supply is shown in Fig. 6(c). The efficiency increases in time, as shown in Fig. 6(d). The efficiency is about 50% at the time the maximum power is being added to the capacitors.

In the simulations, we separately monitored the power delivered to the circuit for both the AC power supply and the DC power supply. The DC power supply was found to not do any work on the circuit, while the AC power supply did all the work. The AC power supply mimics the role of the varying capacitance in Fig. 1(a). This indicates that the energy harvested by the circuit in Fig. 1(a) arises from the work done to rotate the variable capacitor, and not from the DC power supply. A DC voltage offset was added to these AC experiments and resulted in no additional energy harvesting, which further supports the conclusion that the DC source does not contribute to the energy harvested.

In addition to the circuit shown in Fig. 4(a), we also simulated the performance of four more circuit topologies that are shown in Fig. 7. The first is a circuit with a standard four-diode bridge and one storage capacitor, as shown in Fig. 7(a). The second is a circuit with two diodes and one storage capacitor, as shown in Fig. 7(b). The third is a circuit with two diodes and two storage capacitors, as shown in Fig. 7(c). The fourth is a circuit with two transistors and one storage capacitor, as shown in Fig. 7(d). The efficiency of each circuit is shown in Table I. The lowest efficiency comes from



**FIG. 6.** Simulation results. (a) Voltage on  $C_2$ , (b) total power on both capacitors, (c) power delivered to the circuit from the power supply, and (d) efficiency as a function of the cycle number.



**FIG. 7.** AC topologies for maximum efficiency studies. (a) Four-diode bridge with one storage capacitor. (b) Two diodes and one storage capacitor. (c) Two diodes and two storage capacitors. (d) Two transistors and one storage capacitor.

the four-diode bridge circuit. This is due to the high forward resistance of the diodes at these low currents. Because this circuit has four resistive elements, it is less efficient. The circuits with only one storage capacitor are always less efficient. This also shows that the energy can be harvested in the forward bias direction and that the work done comes from rotating the capacitor, and not from the DC power source.

## V. ANALYSIS OF CIRCUITS AND PRINCIPLES OF OPERATION

To fully understand the simulations detailed in this paper, it is helpful to consider how the circuit functions, how it converts kinetic energy into stored electrical charge, and what factors control the efficiency. To begin with, the voltage data  $V_{C_2}(t)$  shown in Fig. 2(a) fit extremely well to Eq. (1), which is the formula for the voltage as a function of time for a charging RC series circuit. When the time

**TABLE I.** Circuit topology simulation results.

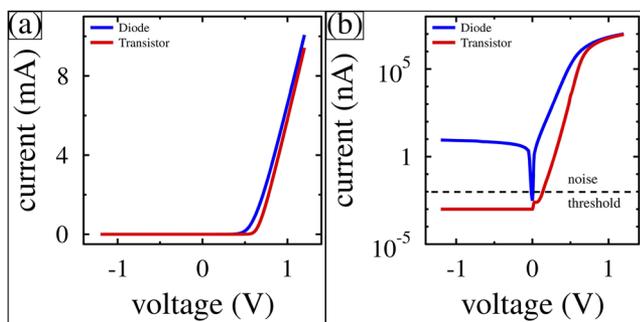
Circuit topology	Efficiency at maximum output power (%)
4 diodes (BAS16HM), 1 storage capacitor	14
2 diodes (BAS16HM), 1 storage capacitor	22
2 diodes (BAS16HM), 2 storage capacitors	22
2 transistors (2N3904), 1 storage capacitor	30
2 transistors (2N3904), 2 storage capacitors	50

constant (819 s) is combined with the value of the storage capacitor (950 nF), the equivalent resistance is 862 M $\Omega$ . The next step is to determine the source of this resistance. Normally, diodes are treated as perfect switches, which display either zero or infinite resistance. However, for low power energy harvesting, the current levels are so minimal that the diode's resistance becomes a significant factor.

To determine this resistance, we measured the IV characteristics of both the diodes and the transistors, as shown in Fig. 8. The current is shown in units of mA and on a linear scale in Fig. 8(a), so both the diode and the transistor appear to be very similar. However, from Fig. 2(b), we know the current is about 10 nA or less. For this current level, the IV characteristics must be viewed on a log scale, as shown in Fig. 8(b). In the forward bias, the diode has 10 nA of current near 0.1 V. This indicates that its resistance is about 10 M $\Omega$ , while the transistor's resistance is closer to 50 M $\Omega$  (at 10 nA). However, because the current flows for only a 20th of the 1 s cycle, the effective resistance is 1000 M $\Omega$ . This explains the origin of the resistance. Next, the origin of the shorter duty cycle shown in Fig. 2(d) must be determined.

To understand the duty cycle, it is helpful to consider a situation in which the charge on the VC is fixed. For the fixed charge, we let  $C_{VC} = 1.0$  nF and  $V_{VC} = 1.0$  V and then  $Q_{VC} = 1.0$  nC. After rotating the VC to have  $C_{VC} = 0.1$  nF, with  $Q_{VC}$  fixed,  $V_{VC}$  increases to 10.0 V, since  $V = Q/C$ . This increase in voltage is the force that does work on the circuit. Thus, as the voltage on the storage capacitor  $C_2$  rises, the charge cannot leave the VC until its voltage rises above the voltage of  $C_2$ . This is the reason the duty cycle becomes shorter, which increases the effective resistance.

Given that the transistor has more resistance than the diode, it seems reasonable to conclude that the diode would be more efficient, as lower resistance minimizes dissipative losses. Yet the efficiency is improved with transistors, as compared to diodes. The explanation for this lies in the reverse bias IV characteristics. As the voltage on  $C_1$  becomes larger in Fig. 1(a), the transistor experiences a larger reverse bias. If the voltage on  $C_1$  is 1 V, for example, then the transistor (or diode) is in the reverse bias at 1 V. From the IV curves shown in Fig. 8(b), it is clear the diode will leak 10 nA of current continuously, while the transistor will leak as much as 10 000 times less. This is the reason for the difference in efficiency. The transistors are more efficient because they are better at keeping the capacitor charged.



**FIG. 8.** Diode and transistor IV characteristics shown on a (a) linear scale and (b) log scale.

One question remains: why are two capacitors better than one for the transistor, but not for the diode. We found that two capacitors are better than one if each cycle (CW and CCW) of the circuit operates independently. As current flows through  $D_1$ , it charges  $C_1$ , and as current flows through  $D_2$ , it charges  $C_2$ . To understand why the diode circuit fails to double the efficiency, it is helpful to consider a situation in which the two storage capacitors are charged to 10 V and then the VC stops turning. The diodes are now in the reverse bias at 10 V, and the current flows backward through the two diodes from  $C_1$  to  $C_2$  and back to  $C_1$ . In fact,  $C_1$  and  $C_2$  are now effectively connected in series, which halves the total storage capacitance of the circuit. Thus, if the voltage on the storage capacitors is too high, current will leak off and lower the efficiency.

For this study, we physically rotate the VC to produce power. However, varying capacitance can be driven by ambient vibrations, as well.<sup>2</sup> For example, the circuit presented in our study could harvest energy from the varying capacitance of a MEMS device. In addition, this entire circuit could be built on a silicon integrated circuit and duplicated for increased power. It has also been demonstrated that two-dimensional materials are extremely flexible and vibrate under the slightest influence.<sup>5,30</sup> Their capacitance can also be controlled using a DC bias voltage.<sup>31,32</sup> These materials could enable new low power applications utilizing one of these energy harvesting circuit designs.

## VI. SUMMARY

Low power energy harvesting circuits, which utilize variable capacitance as a source of power, have been investigated. Five different circuit topologies were simulated, and the most efficient one was experimentally tested. The most efficient circuit utilizes two transistors for rectification and two storage capacitors. The storage capacitors can be charged to any voltage set by a DC power supply. The source of power comes from the driving force behind the varying capacitance and not from the DC power supply. The maximum output power for the circuit was 10 nW, and at that power, the efficiency was 50%.

## ACKNOWLEDGMENTS

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## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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